Electronic Version
Stylesheet Version v1.1.1

SCAN CHAIN MODIFICATION FOR REDUCED LEAKAGE

Abstract

A leakage power control vector is loaded into existing test scan chain elements for application to circuit elements of a circuit in which the leakage currents are to be controlled. The vector is designed to configure the circuit elements into states in which leakage currents are reduced. A multiplexer selects the power control vector for loading into the scan chain elements, and a clock generator clocks the configuration vector into the scan chain elements. A sleep mode detector may be provided to configure the multiplexer to select the power control vector and to operate the clock generator to clock the power control vector into the scan chain elements when a sleep mode of the circuit is detected.